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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/225,388	01/05/1999	DAVID W SMITH	2000.002500	2528

23720 7590 07/17/2003

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EXAMINER	
NGUYEN, TOAN D	
ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 07/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/225,388	SMITH, DAVID W
	Examiner	Art Unit
	Toan D Nguyen	2665

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-18,20-28 and 30-35* is/are rejected.

7)☒ Claim(s) *7,19 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 9, 23-24, 31-32 and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by McKaughan et al. (U.S. Patent 5,802,305).

For claims 1, McKaughan et al. disclose system for remotely waking a sleeping computer in power down state by comparing incoming packet to the list of packets storing on network interface card comprising:

receiving a set of data signals from an external data source (figure 4, col. 8 lines 45-47);

decoding said received set of data signals (col. 8 lines 47-50);

extracting a destination address from said set of data signals (col. 8 lines 47-50);

comparing said destination address extracted from said data signals to a known data value (col. 8 lines 52-54);

determining whether said received data signals should be received by a host circuitry based upon said comparison of said destination address extracted from said data signals to a known data value (col. 8 lines 54-58);

generating at least one status signal alerting said host circuitry of said determination that said received data signals should be received by said host circuitry (col. 8 lines 59-64); and

waking up said host circuitry from a sleep mode upon a determination that said received set of data is addressed to said host circuitry (figure 4, col. 8 lines 59-64).

For claims 2 and 24, McKaughan et al. disclose set of data signal received is data packet that is in a serial data format, over a network line (col. 8 lines 45-47).

For claims 9 and 31, McKaughan et al. disclose wherein said method of waking up said host circuitry further comprises generating a status signal alerting said host that a address match has been found (figure 4, col. 59-62).

For claim 23, the claim is directed to the same subject matter as in claim 1. Therefore, it is subject to the same rejection.

For claim 32, McKaughan et al. disclose system for remotely waking a sleeping computer in power down state by comparing incoming packet to the list of packets storing on network interface card comprising:

receiving a data signal (figure 4, col. 8 lines 45-47);

extracting a destination address based upon said data signal to determine whether a host circuitry is being addressed by comparing said destination address to a predetermined address; (col. 8 lines 47-54);and

waking up a host circuitry from a sleep mode based upon said determination that said host circuitry is being addressed (figure 4, col. 8 lines 59-64).

For claim 34, the claim is directed to the same subject matter as in claim 32. Therefore, it is subject to the same rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3-6, 8, 10-18, 20-22, 25-28, 30, 33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over McKaughan et al. (U.S. Patent 5,802,305) in view of Dailey et al. (U.S. Patent 5,487,181).

For claims 3-6, 8, 25-28, 30 and 33, McKaughan et al. do not disclose step of detecting a size of said received set of data signal and decoding said received set of data signals, includes:

converting said serial data packet into a parallel data format;

extracting a word clock from said received data packet;

incrementing a member held by said counter, said word clock generating a word count;

inputting said converted parallel format data into a plurality of comparators;

using said word count to address data stored in a memory circuitry; and

inputting a set of data signals from said memory circuitry into an appropriate comparator.

In an analogous art, Dailey et al. disclose:

converting said serial data packet into a parallel data format (col. 11 lines 46-47);

extracting a word clock from said received data packet (col. 11 lines 49-51);

incrementing a member held by said counter, said word clock generating a word count (col. 12 line 26);

inputting said converted parallel format data into a plurality of comparators (col. 11 lines 56-60);

using said word count to address data stored in a memory circuitry (col. 12 lines 24-27); and

inputting a set of data signals from said memory circuitry into an appropriate comparator (col. 11 lines 56-60).

Dailey et al. disclose further wherein said act of extracting a destination address from said set of data signals further comprises slicing said parallel data such that at least one destination address data word is generated (col. 11 lines 46-53 as set forth in claims 4 and 26); performing a comparison function upon said converted, parallel set of data signals, and said set of data from said memory circuitry (col. 11 lines 46-60), generating a digital comparator status signal in response of said performance of comparator function; and clocking in said digital comparator data signal into a register (col. 11 line 61 to col. 12 line 7 as set forth in claims 5 and 27); determining whether said received data signals should be received by a host circuitry further comprises latching all output of said plurality of comparators into a digital logic circuitry (col. 12 lines 8-11 as set forth in claims 6 and 28); performing an OR function upon all said latched output of said comparator (figure 9, col. 13 lines 14-17 as set forth in claims 8 and 30).

One skilled in the art would have recognized a shift register to convert the received data from a serial format to a parallel format to use the teachings of Dailey et al. in the system of McKaughan et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time invention, to use the shift register as taught by Dailey et al. in McKaughan et al.'s system with the motivation being to support two basic modes of operation: normal and match (col. 11 lines 47-49).

For claims 10-18, 20-22 and 35, McKaughan et al. disclose system for remotely waking a sleeping computer in power down state by comparing incoming packet to the list of packets storing on network interface card, comprising:

a counter (col. 6 line 43);

a host circuitry interface capable of transmitting and receiving data from a host circuitry said host circuitry enter a wake up state from a sleep mode based upon decoded address data received by said host circuitry (figure 1, col. 6 lines 26-29);

a memory circuitry (figure 2, col. 6 line 42-43);

a mask circuitry (col. 8 line 48);

However, McKaughan et al. do not disclose:

a data formatter;

a clock divider;

a plurality of comparators;

a digital logic circuitry;

a plurality of status registers and a plurality of clocked registers.

In an analogous art, Dailey et al. disclose:

a data formatter (col. 11 lines 46-47);

a clock divider (col. 10 lines 34-36);

a plurality of comparators (col. 11 lines 59-60);

a digital logic circuitry (figure 9);

a plurality of status registers and a plurality of clocked registers (col. 10 lines 51-52).

Dailey et al. disclose further formatter comprises of a serial to parallel converter and a data end detector that are capable of converting a serial stream of data into parallel data words and detecting an end of a data stream (col. 11 lines 46-55 as set forth in claim 11); memory circuitry comprises of a memory element and a memory data access logic (figure 7, col. 12 lines 20-29 as set forth in claims 13 and 14); memory data access logic is coupled with said host interface such that data can be sent to and retrieved from said memory elements (figure 6, col. 11 lines 46-47 as set forth in claims 15 and 22); and comparators are coupled with said data formatter such that said comparators receive parallel formatted data from said data formatter (col. 11 lines 46-60 as set forth in claims 16-18 and 20-21).

One skilled in the art would have recognized a shift register to convert the received data from a serial format to a parallel format to use the teachings of Dailey et al. in the system of McKaughan et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time invention, to use the shift register as taught by Dailey et al. in McKaughan et al.'s system with the motivation being to support two basic modes of operation: normal and match (col. 11 lines 47-49).

Allowable Subject Matter

5. Claims 7, 19 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response To Arguments

6. Applicant's arguments filed on May 05, 2003 have been fully considered but are moot in view of the new ground(s) of rejection.

Contact Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan D Nguyen whose telephone number is 703-305-0140. The examiner can normally be reached on Monday- Friday (7:00AM-4:30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Huy Vu can be reached on 703-308-6602. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

TN
T.N.